THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHEN J. AMURO
and PAUL J. GIORGIO

Appeal No. 97-1263
Application No. 08/219,552[1]

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-10. The appellants filed an amendment after final rejection on April 25, 1996, which was entered. We reverse.

[1] The application, entitled "SCSI Controller with Target Status Retrieval," was filed March 29, 1994.

BACKGROUND

The appellants' invention is a system for interfacing a plurality of host processors to a plurality of Small Computer System Interface (SCSI) peripheral devices, i.e., SCSI targets, via a single SCSI initiator. Status data, i.e., ATTENTION DATA, from each target are written to a memory from which the host processors can read the data. The memory contains a separate address space for each combination of processor and target.

Claim 1, which is representative for our purposes, follows:

> 1. A system including a small computer system interface comprising:
>
> a plurality of host processors;
>
> a controller connected to each of said plurality of host processors, said controller including an interconnection of only one SCSI initiator, at least one host adapter, a microprocessor and a memory;
>
> a plurality of SCSI targets with each of said plurality of SCSI targets connected to said controller;
>
> said each of said host processors having issuing and receiving means for issuing separate commands to designated SCSI targets through said controller and

> for receiving information in response to said commands from said designated SCSI targets through said controller;
>
> said controller further having first processing means for processing said separate commands from each of said host processors to said designated members of said SCSI targets, and second processing means for processing said information from said designated members of said SCSI targets to said each of said plurality of host processors;
>
> each of said designated members of said SCSI targets having generating means for generating said information in response to said commands, said information signifying if a UNIT ATTENTION condition exists; and
>
> said controller further having first storage means for storing said information as ATTENTION DATA from each of said plurality of SCSI targets for each of said plurality of host processors, when said UNIT ATTENTION condition exists, said first storage means further having a separate memory location for each combination of said SCSI targets and said host processors. (Spec. at 16-17.)

The references relied on by the patent examiner in rejecting the claims follow:

Fischer 4,783,730 Nov. 8, 1988

American National Standards Institute (ANSI), ANSI X3.131-1986, “Small Computer System Interface(SCSI)” pp. 26, 51-71, 80-82, 185-86, 194-99, 208-09 (June 23, 1986).

Claims 1-10 stand rejected under 35 U.S.C. § 103 as obvious over Fischer in view of ANSI. (Examiner's Answer at 3.) Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the appeal and reply briefs and the examiner's answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. We also considered the appellants' and examiner's arguments. After considering the record before us, it is our view that the evidence and level of skill in the art would not have suggested to one of ordinary skill in the art the invention of claims 1-10. Accordingly, we reverse.

We begin our consideration of the obviousness of the claims by recalling that in rejecting claims under 35 U.S.C. § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. A prima facie case is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

If the burden of establishing a prima facie case is met, the burden of coming forward with evidence or argument shifts

to the appellant. After evidence or argument is submitted by the appellant in response, patentability is determined on the totality of the record, by a preponderance of evidence with due consideration to persuasiveness of argument. In reviewing the examiner's decision on appeal, the Board of Patent Appeals and Interferences (Board) must weigh all the evidence and argument. An observation by the Board that the examiner made a prima facie case is not improper, if the ultimate determination of patentability is made on the entire record. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). With this in mind, we consider the examiner’s rejection.

The examiner begins the rejection by observing that Fischer describes a system comprising host processors; a controller, which is “a only a SCSI initiator,” (Examiner’s Answer at 3); and SCSI targets. (Id. at 4.) Next, the examiner describes the reference as follows.

> Fischer on column 2, lines 35-59, describes how the processors and targets communicate between each other. There is a Mailbox or storage means given to each processor modules (see column 4, lines 53-62)

> and I/0 adaptors with Queue Descriptors for each I/0 device in the Mailboxes (see columns 5-7) for storing ATTENTION DATA (see Module Attention and Device Attention on columns 7-8 and 29, line 45 et seq.) when a UNIT ATTENTION condition exists. The commands to be sent and received between the hosts and targets such as ATTENTION DATA, CHECK CONDITION, giving a warning, resending the warning, REQUEST SENSE, getting the sense key, checking UNIT ATTENTION are SCSI standard commands which are followed by Fischer as shown on column 24, lines 53-54. Fischer teaches the basic structure of the inventive system fo [sic, for] claims 1-10, but doesn't provide all of the details of SCSI operation attributed to the various elements as claimed by the Applicant. Fischer describes that when the controller detects an error during a device operation the Queue Descriptor which is in memory for each decvice [sic] is checked as shown on column 32, lines 42-64. Fischer describes that EACH HOST has memory allocated for EACH TARGET for SCSI commands. The commands to be sent and received between the hosts and targets such as ATTENTION DATA, CHECK CONDITION, giving a warning, resending the warning, REQUEST SENSE, getting the sense key, checking UNIT ATTENTION are SCSI standard commands. (Id.)

The examiner also opines that the claimed memory structure "would appear to be equivalent to the structure disclosed by Fischer at column 2, lines 44-48." (Supplemental Examiner's Answer at 2.) The examiner reasons, "[s]ince Fischer suggests SCSI operation in accordance with the ANSI standard, the artisan would have ben [sic, been] motivated to implement SCSI

operation in accordance with this standard." (Examiner's Answer at 4-5.)

Regarding ANSI, the examiner asserts, "[t]he SCSI standard teaches how a SCSI initiator works with just one memory unit connected to one host which is an equivalent structure to that described by Applicant. See SCSI standard sections 6, 6.1.3, 7.1.1-3, 7.1.5-6, pp. 26, 51-71, 80-82, 185-186, 194-199, 208-209. The referenced sections teach the operation of the elements as claimed by the Applicant." (Id. at 5.)

The examiner ends the rejection by concluding that it would have been obvious to one of ordinary skill in the art at the time of invention "to provide the apparatus disclosed and claimed by Applicant in claims 1-9 to operate in accordance with the ANSI SCSI stsndard [sic, standard] in the system described by Fischer, since Fischer leaves details of SCSI operation unsaid and explicitly suggests that the ANSI SCSI standard be followed." (Id.)

We observe that the examiner satisfied the burden of establishing a prima facie of obviousness. Accordingly, the burden of coming forward with evidence or argument was shifted to the appellants. They came forward with argument. We now consider their argument.

The appellants' argument focuses on the storage means of claim 1. The claim recites in pertinent part a "first storage means for storing said information as ATTENTION DATA from each of said plurality of SCSI targets for each of said plurality of host processors, ... said first storage means further having a separate memory location for each combination of said SCSI targets and said host processors." (Spec. at 17.) The appellants' argument regarding the storage means follows.

> Fischer recites a Mailbox for each processor module and each adapter module, but does not recite a Mailbox for each combination of processor module and adapter module. Nowhere does Fischer's memory architecture allow for Appellants' unique means for storing ATTENTION DATA from each target for each host processor with a separate memory location for each combination of targets and processors, as recited in Appellants' claim 1. Neither the SCSI standard nor Fischer, alone or in combination, appear to teach such a storing means. Therefore, it would not have been obvious to use Fischer in

> combination with the SCSI standard to obtain such a result as disclosed by Appellants. (Reply Br. at 2-3.)

In response, the examiner opines that the claimed storage means "would appear to be equivalent to the structure disclosed by Fischer at column 2, lines 44-48." (Supplemental Examiner's Answer at 2.) The passage cited by the examiner states that "[t]he method of the present invention utilizes a multilevel communication structure. The first memory structure, designated a Mailbox, is established for holding data for communicating

module information between each processor and each I/O adapter." Col. 2, ll. 44-48.

A rejection based on section 103 must rest on a factual basis. An examiner has the initial duty of supplying the factual basis for any rejection he advances. He may not resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in the factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). In this case, we find that the cited passage is ambiguous, at best. By itself, the passage possibly could be interpreted as teaching the claimed separate memory location for each combination of SCSI target and host processors. In view of the ambiguity of the passage's language, however, such an interpretation amounts to speculation.

As a whole, moreover, Fischer belies this interpretation. The reference specifically teaches that there is one Mailbox for each central processor module 20 and I/O adapter module 22. Col. 4, ll. 61-62. In contrast to the claimed invention, there are no mailboxes for the I/O devices, which the examiner

maps to the claimed targets. (Examiner's Answer at 4.) Also in contrast, mailboxes are not allocated for combinations of processor modules and adapter modules. There is nothing in the reference nor in ANSI, furthermore, that would have suggested replacing Fischer's memory structure with the claimed storage.

For the foregoing reasons, we find that Fischer and ANSI neither teach nor would have suggested the storage means as in independent claim 1 and its dependent claims 2-10. Therefore, we reverse the rejection of claims 1-10 under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-10 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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